IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (currently amended) A method for reliably transmitting data between microprocessors, comprising:

selecting a data packet stored in memory associated with a first microprocessor to be transmitted from ~~a~~ the first microprocessor to a second microprocessor;

establishing a pointer region configured to indicate an address of the data packet in the memory;

appending a first value derived from the data packet to the data packet;

transmitting the data packet to a second microprocessor;

comparing the first value to a second value derived from the data packet received by the second microprocessor;

if the second value is different than the first value then the method includes,

transmitting a signal to the pointer region for re-transmission of the data packet; and

re-transmitting the data packet from the memory.

2. (original) The method of claim 1, wherein the method operation of appending a first value derived from the data packet to the data packet includes,

calculating a cyclic redundancy check (CRC) to append with the data.

3. (original) The method of claim 1, wherein the method operation of appending a first value derived from the data packet to the data packet includes,

performing a parity check on the data packet; and

if the parity check locates an error, then the method includes,

corrupting a CRC value associated with the data packet.

4. (original) The method of claim 3, wherein the method operation of transmitting a signal to the pointer region for re-transmission of the data packet includes,

communicating a memory address of the data packet to a scheduling module; and

directing selection logic to select the data packet for re-transmission.

5. (original) The method of claim 1, wherein the method operation of establishing a pointer region configured to indicate an address of the data packet in the memory includes,

defining a plurality of retry pointers within the pointer region; and

associating one of the plurality of retry pointers with a memory address of the data packet.

6. (original) The method of claim 1, wherein the pointer region includes a plurality of retry pointers, each of the plurality of retry pointers being 11 bit pointers.

7. (original) A microchip configured to reliably transmit data, comprising:

a memory region for storing data;

a selection module configured to select a portion of the data from the memory region for transmission;

an error checking module configured to calculate a value derived from the selected portion of the data prior to transmission of the selected portion;

a pointer region including a plurality of object pointers, one of the plurality of object pointers associated with an address of the portion of the data, wherein the one of the plurality of object pointers is configured to receive a signal indicating an error associated with the transmission of the selected portion of the data;

a scheduler module in communication with each of the plurality of object pointers, wherein the scheduler module is configured to schedule re-transmission of the selected portion of the data from the memory in response to the signal indicating the error being received by the one of the plurality of object pointers.

8. (original) The microchip of claim 7, wherein the error checking module is configured to cause the signal to be generated by an external error checking module when an error associated with data is detected.

9. (original) The microchip of claim 7, wherein the signal is a retry signal and the one of the object pointers is an 11 bit retry pointer.

10. (original) The microchip of claim 7, further comprising:

a single buffer configured to receive the selected portion of the data; and

a serializer buffer capable of serializing data for transmission.

11. (original) The microchip of claim 7, wherein each the plurality of object pointers is an 11 bit retry pointer.

12. (original) The microchip of claim 7, wherein the scheduler module is configured to override the selection module to schedule re-transmission of the selected portion of the data from the memory.

13. (original) The microchip of claim 7, wherein the error checking module is configured to perform both a cyclic redundancy check and a parity check on the selected portion of the data from the memory.

14. (original) A system providing reliable link data flow between microchips;

a first microchip including a memory capable of storing a data packet, the first microchip further including,

a pointer associated with a memory address of the data packet;

a selection logic module in communication with the memory, the selection logic module configured to select the data packet for transmission from the memory; and

an error checking module configured to calculate a first value derived from the data packet prior to transmission of the data packet from the first microchip;

a serial link; and

a second microchip in communication with the first microchip through the serial link, the second microchip including an error verifying module configured to calculate a second value derived from the data packet received from the first microchip, the error verifying module further configured compare the second value to the first value, wherein if the first value and the second value are different the error verifying module transmits a signal to the pointer causing the data packet to be re-transmitted to the second microchip from the memory of the first microchip.

15. (original) The system of claim 14, wherein the pointer is an 11 bit pointer.

16. (original) The system of claim 14, wherein the first microchip further comprises:

a scheduling module in communication with the pointer, the scheduling module configured to override the selection module for re-transmission of the data packet.

17. (original) The system of claim 14, wherein the first microchip further comprises:

a buffer configured to hold the data packet; and

a serial buffer in communication with the buffer, the serial buffer configured to serialize data for transmission.

18. (original) The system of claim 14, wherein the error checking module is configured to perform both a cyclic redundancy check (CRC) and a parity check on the data packet.

19. (original) The system of claim 18, wherein the error checking module is further configured to corrupt the CRC when the parity check detects an error associated with the data packet.